CLAIMS

1. A controller for executing an application program to process control information related to control elements comprising:

a. a plurality of main processor modules each of which runs the application program;

b. at least one input/output module for receiving and sending control information to said control elements, communicating with each main processor module;

c. at least one communication module communicating external signals to said plurality of main processor modules;

d. a time synchronizing system for synchronizing the time clocks of said main processor modules;

e. a voting system which exchanges information between selected ones of said main processor modules of said plurality of main processor modules and compares the information in each main processor module with the information in other selected ones of said main processor modules;

f. a selection system which determines which of said plurality of main processor modules is a selected one of said plurality of main processor modules which is used to compare information in each main processor module;

g. a plurality of separate housings for enclosing electronic circuit boards representing said modules, having a common physical characteristics for receiving said electronic circuit boards and providing housing electrical connectors;

h. at least one base plate circuit board for mounting each module which provides base plate electrical connectors for receiving the housing electrical connectors; and

i. a common rail system for mounting of said at least one base plate circuit board and providing electrical connections to each of said housings.

2. A controller as described in claim 1 wherein there are a plurality of base plate circuit boards, selected ones of said base plate circuit boards receiving said housing for said main

processor modules, other selected ones of said base plate circuit boards receiving said housing for said at least one input/output module, and still other selected ones of said base plate circuit boards receiving said housing for said at least one communication module.

3. A controller as described in claim 1 wherein each of said plurality of housings includes a mounting fastener attached to said housing which is used to mount said housing to said baseplate circuit board and remove said housing from said base plate circuit board.

4. A controller as described in claim 3 wherein said fastener is an elongated screw which is rotatable attached to said housing along its length such that when the screw is rotated in a first direction the housing electrical connectors are pulled into engagement with said base plate electrical connectors and when turned in an opposite direction pulls said housing electrical connectors out of engagement with said base plate electrical connectors.

5. A controller as described in claim 3 further comprising a sensor for sensing a change in position of said fastener and a module remove detector system for indicating that the fastener position has changed.

6. A controller for executing an application program to process control information related to control elements comprising:

a. a plurality of main processor modules each of which runs the application program;

b. at least one input/output module for receiving and sending control information to said control elements communicating with each main processor module;

c. a time synchronizing system for synchronizing the time clocks of said main processor modules;

d. a voting system which exchanges information between selected ones of said main processor modules of said plurality of main processor modules and compares the information in each selected main processor module with the information in other selected ones of said main processor modules;

e. a selection system which determines which of said plurality of main processor modules is a selected one of said plurality of main processor modules which is used to compare information in each main processor module;

f. a channel transmission validity testing system;

g. a plurality of separate housings for enclosing electronic circuit boards representing said modules, having a common physical characteristics for receiving said electronic circuit boards and providing housing electrical connectors;

h. at least one base plate circuit board for mounting each module which provides base plate electrical connectors for receiving the housing electrical connectors; and

i. a common rail system for mounting of said at least one base plate circuit board and providing electrical connections to each of said housings.

7. A controller as described in claim 6 wherein there are a plurality of base plate circuit boards, selected ones of said base plate circuit boards receiving said housing for said main processor modules, and other selected ones of said base plate circuit boards receiving said housing for said at least one input/output module.

8. A controller as described in claim 6 wherein said housing includes a mounting fastener attached to said housing which is used to mount and remove said housing from said base plate circuit board by manipulation of said fastener.

9. A controller as described in claim 8 wherein said fastener is an elongated screw which is rotatable attached to said housing along its length such that when the screw is rotated in a first direction the housing electrical connectors are pulled into engagement with said base plate electrical connectors and when turned in an opposite direction pulls said housing electrical connectors out of engagement with said base plate electrical connectors.

10. A controller as described in claim 8 further comprising a sensor for sensing a change in position of said fastener and a module remove detector system for indicating that the fastener position has changed.

11. A controller for executing an application program to process control information related to control elements comprising:

a. a plurality of main processor modules each of which runs the application program;

b. at least one input/output module for receiving and sending control information to control elements, communicating with each main processor module;

c. at least one communication module communicating external signals to said plurality of main processor modules;

d. a time synchronizing system for synchronizing the time clocks of said main processor modules;

e. a voting system which exchanges information between selected ones of said main processor modules of said plurality of modules and compares the information in each main processor module with the information in other selected ones of said main processor modules;

f. a selection system which determines which of said plurality of main processor modules is a selected one of said plurality of main processor modules which is used to compare information in each main processor module;

g. a plurality of separate housings for enclosing electronic circuit boards representing said modules, having a common physical characteristics for receiving said electronic circuit boards and providing housing electrical connectors;

h. at least one base plate circuit board for mounting each module which provides base plate electrical connectors for receiving the housing electrical connectors; and

i. a common rail system for mounting of said at least one base plate circuit board and providing electrical receptacles to each of said housings.

12. A controller as described in claim 11 wherein there are a plurality of base plate circuit boards, selected ones of said base plate circuit boards receiving said housing for said main processor modules, other selected ones of said base plate circuit boards receiving said housing for said at least one input/output module, and still other selected ones of said base plate circuit boards receiving said housing for said at least one communication module.

13. A controller as described in claim 11 wherein said housing includes a mounting fastener attached to said housing which is used to mount and remove said housing from said base plate circuit board.

14. A controller as described in claim 13 wherein said fastener is an elongated screw which is rotatable attached to said housing along its length such that when the screw is

rotated in a first direction the housing electrical connectors are pulled into engagement with said base plate electrical connectors and when turned in an opposite direction pulls said housing electrical connectors out of engagement with said base plate electrical connectors.

15. A controller as described in claim 13 further comprising a sensor for sensing a change in position of said fastener and a module remove detector system for indicating that the fastener position has changed.

16. A controller for executing an application program to process control information related to control elements comprising:

a. a plurality of main processor modules each of which runs the application program;

b. at least one input/output module for receiving and sending control information to control elements communicating with each main processor module;

c. a time synchronizing system for synchronizing the time clocks of said main processor modules;

d. a voting system which exchanges information between selected ones of said main processor modules of said plurality of modules and compares the information in each main processor module with the information in other selected ones of said main processor modules;

e. a selection system which determines which of said plurality of main processor modules is a selected one of said plurality of main processor modules which is used to compare information in each main processor module;

f. a plurality of separate housings for enclosing electronic circuit boards representing said modules, having a common physical characteristics for receiving said electronic circuit boards and providing housing electrical connectors;

g. at least one base plate circuit board for mounting each module which provides base plate electrical receptacles for receiving the housing electrical connectors; and

h. a common rail system for mounting of said at least one base plate circuit board and providing electrical connections to each of said housings.

17. A controller as described in claim 16 wherein there are a plurality of base plate circuit boards, selected ones of said base plate circuit boards receiving said housing for said main processor modules, other selected ones of said base plate circuit boards receiving said housing for said at least one input/output module, and still other selected ones of said base plate circuit boards receiving said housing for said at least one communication module.

18. A controller as described in claim 16 wherein said housing includes a mounting fastener attached to said housing which is used to mount and remove said housing from said base plate circuit board.

19. A controller as described in claim 18 wherein said fastener is an elongated screw which is rotatable attached to said housing along its length such that when the screw is rotated in a first direction the housing electrical connectors are pulled into engagement with said base plate electrical connectors and when turned in an opposite direction pulls said housing electrical connectors out of engagement with said base plate electrical connectors.

20. A controller as described in claim 18 further comprising a sensor for sensing a change in position of said fastener and a module remove detector system for indicating that the fastener position has changed.

21. A controller for executing an application program to process control information related to control elements comprising:

a. a plurality of main processor modules each of which runs the application program;

b. a time synchronizing system for synchronizing the time clocks of said main processor modules;

c. a voting system which exchanges information between selected ones of said main processor modules of said plurality of modules and compares the information in each main processor module with the information in other selected ones of said main processor modules;

d. a selection system which determines which of said plurality of main processor modules is a selected one of said plurality of main processor modules which is used to compare information in each main processor module;

e. a plurality of separate housings for enclosing electronic circuit boards representing said modules, having a common physical characteristics for receiving said electronic circuit boards and providing housing electrical connectors;

f. at least one base plate circuit board for mounting each module which provides base plate electrical connectors for receiving the housing electrical connectors; and

g. a common rail system for mounting of said at least one base plate circuit board and providing electrical connections to each of said housings.

22. A controller as described in claim 21 wherein there are a plurality of base plate circuit boards, selected ones of said base plate circuit boards receiving said housing for said main processor modules, other selected ones of said base plate circuit boards receiving said housing for said at least one input/output module, and still other selected ones of said base plate circuit boards receiving said housing for said at least one communication module.

23. A controller as described in claim 21 wherein said housing includes a mounting fastener attached to said housing which is used to mount and remove said housing from said base plate circuit board.

24. A controller as described in claim 23 wherein said fastener is an elongated screw which is rotatable attached to said housing along its length such that when the screw is rotated in a first direction the housing electrical connectors are pulled into engagement with said base plate electrical connectors and when turned in an opposite direction pulls said housing electrical connectors out of engagement with said base plate electrical connectors.

25. A controller as described in claim 23 further comprising a sensor for sensing a change in position of said fastener and a module remove detector system for indicating that the fastener position has changed.

26. A controller as described in claim 21 further comprising at least one input/output module for receiving and sending control information to control elements in said control system communicating with each of said plurality of main processor modules.

27. A controller as described in claim 21 further comprising at least one communication module receiving communicating external signals to of said plurality of main processor modules.

28. A controller as described in claim 21 further comprising:

a. at least one input/output module for receiving and sending control information to control elements in said control system communicating with each of said plurality of main processor modules; and

b. at least one communication module for sending and receiving external signals communicating with each of said plurality of main processor modules.

29. A control system platform for executing an application program to process control information related to control elements comprising:

a. a plurality of main processor modules each of which runs the application program;

b. at least one input/output module for receiving and sending control information to control elements communicating with each main processor module;

c. at least one communication module communicating external signals to said plurality of main processor modules;

d. a time synchronizing system for synchronizing the time clocks of said main processor modules;

e. a voting system which exchanges information between selected ones of said main processor modules of said plurality of modules and compares the information in each main processor module with the information in other selected ones of said main processor modules;

f. a selection system which determines which of said plurality of main processor modules is a selected one of said plurality of main processor modules which is used to compare information in each main processor module;

g. a plurality of separate housings for enclosing electronic circuit boards representing said modules, having a common physical characteristics for

receiving said electronic circuit boards and providing housing electrical connectors;

h. at least one base plate circuit board for mounting each module which provides base plate electrical connectors for receiving the housing electrical connectors; and

i. a common rail system for mounting of said at least one base plate circuit board and providing electrical connections to each of said housings.

30. A control system platform described in claim 29 wherein there are a plurality of base plate circuit boards, selected ones of said base plate circuit boards receiving said housing for said main processor modules, other selected ones of said base plate circuit boards receiving said housing for said at least one input/output module, and still other selected ones of said base plate circuit boards receiving said housing for said at least one communication module.

31. A control system platform as described in claim 29 wherein said housing includes a mounting fastener attached to said housing which is used to mount and remove said housing from said base plate circuit board.

32. A control system platform as described in claim 29 wherein said fastener is an elongated screw which is rotatable attached to said housing along its length such that when the screw is rotated in a first direction the housing electrical connectors are pulled into engagement with said base plate electrical connectors and when turned in an opposite direction pulls said housing electrical connectors out of engagement with said base plate electrical connectors.

33. A control system platform as described in claim 29 further comprising a sensor for sensing a change in position of said fastener and a module remove detector system for indicating that the fastener position has changed.

34. A control system platform for executing an application program to process control information related to control elements comprising:

a. a plurality of main processor modules each of which runs the application program;

b. at least one input/output module for receiving and sending control information to control elements communicating with each main processor module;

c. a time synchronizing system for synchronizing the time clocks of said main processor modules;

d. a voting system which exchanges information between selected ones of said main processor modules of said plurality of modules and compares the information in each main processor module with the information in other selected ones of said main processor modules;

e. a selection system which determines which of said plurality of main processor modules is a selected one of said plurality of main processor modules which is used to compare information in each main processor module;

f. a plurality of separate housings for enclosing electronic circuit boards representing said modules, having a common physical characteristics for receiving said electronic circuit boards and providing housing electrical connectors;

g. at least one base plate circuit board for mounting each module which provides base plate electrical connectors for receiving the housing electrical connectors; and

h. a common rail system for mounting of said at least one base plate circuit board and providing electrical connections to each of said housings.

35. A control system platform as described in claim 34 wherein there are a plurality of base plate circuit boards, selected ones of said base plate circuit boards receiving said housing for said main processor modules, other selected ones of said base plate circuit boards receiving said housing for said at least one input/output module, and still other selected ones of said base plate circuit boards receiving said housing for said at least one communication module.

36. A control system platform as described in claim 34 wherein said housing includes a mounting fastener attached to said housing which is used to mount and remove said housing from said base plate circuit board.

37. A control system platform as described in claim 36 wherein said fastener is an elongated screw which is rotatable attached to said housing along its length such that when the screw is rotated in a first direction the housing electrical connectors are pulled into

engagement with said base plate electrical connectors and when turned in an opposite direction pulls said housing electrical connectors out of engagement with said base plate electrical connectors.

38. A control system platform as described in claim 36 further comprising a sensor for sensing a change in position of said fastener and a module remove detector system for indicating that the fastener position has changed.

39. A control system platform as described in claim 34 wherein there are a plurality of base plate circuit boards, selected ones of said base plate circuit boards receiving said housing for said main processor modules, other selected ones of said base plate circuit boards receiving said housing for said at least one input/output module, and still other selected ones of said base plate circuit boards receiving said housing for said at least one communication module.

40. A control system platform as described in claim 34 wherein said housing includes a mounting fastener attached to said housing which is used to mount and remove said housing from said base plate circuit board.

41. A control system platform as described in claim 36 wherein said fastener is an elongated screw which is rotatable attached to said housing along its length such that when the screw is rotated in a first direction the housing electrical connectors are pulled into engagement with said base plate electrical connectors and when turned in an opposite direction pulls said housing electrical connectors out of engagement with said base plate electrical connectors.

42. A control system platform as described in claim 36 further comprising a sensor for sensing a change in position of said fastener and a module remove detector system for indicating that the fastener position has changed.

43. A control system platform as described in claim 34 further comprising at least one input/output module for receiving and sending control information to control elements in said control system communicating with each of said plurality of main processor modules.

44. A control system platform as described in claim 34 further comprising at least one communication module receiving communicating external signals to of said plurality of main processor modules.

45. A control system platform as described in claim 34 further comprising:

a. at least one input/output module for receiving and sending control information to control elements in said control system communicating with each of said plurality of main processor modules; and

b. at least one communication module for sending and receiving external signals communicating with each of said plurality of main processor modules.

46. A computer-based control system for executing an application program to process control information related to control elements comprising:

a. a plurality of main processor modules each of which runs the application program;

b. at least one input/output module for receiving and sending control information to control elements communicating with each main processor module; and

c. a time synchronizing system for synchronizing the time clocks of said main processor modules.

47. A computer-based control system as described in claim 46 wherein said time synchronization system includes rendezvous signals are sent during a scan cycle.

48. A computer control system as described in claim 46 further comprising at least one communication module for communicating with said main processor modules and external signals.

49. A computer control system as described in claim 48 wherein there are a plurality of communication modules each module communicating independently with said main processor modules and said input/output module.

50. A computer control system for executing an application program to process control information related to control elements comprising:

a. a plurality of main processor modules each of which runs the application program;

b. at least one input/output module for receiving and sending control information to control elements communicating with each main processor module;

c. a time synchronizing system for synchronizing the time clocks of said main processor modules;

d. a voting system which exchanges information between selected ones of said main processor modules of said plurality of modules and compares the information in each main processor module with the information in other selected ones of said main processor modules;

e. a selection system which determines which of said plurality of main processor modules is a selected main processor module which is used to compare information in each main processor module;

f. a plurality of separate housings for enclosing electronic circuit boards representing said modules, having a common physical characteristics for receiving said electronic circuit boards;

g. a common rail system for mounting of said housings and providing electronic connections to each of said housings;

h. apparatus for sending a rendezvous signal to all other main processor modules;

i. apparatus for receiving a rendezvous signal form all other main processor modules;

j. a system for determining the clocking midpoint of all processor signals;

k. a clock update apparatus which sends update signals to the clock to increase the clock rate if slower than the clocking midpoint; and

l. a clock update apparatus which sends update signals to the clock to decrease the clock rate if faster than the clocking midpoint.

51. A control system platform for executing a control system program for managing a control system and evaluating the accuracy of information related to said control system, said platform comprising:

a. a plurality of main processor modules, each executing a copy of said application program;

b. at least one field input/output module communicating with each main processor module;

c. a voting system for comparing information between said main processor modules; and

d. a restoring system for restoring valid information for access by said main processor modules.

52. A control system platform as described in claim 51 wherein said information is selected from the group consisting of:

a. program code,

b. fault detection information,

c. sensor information,

d. command information,

e. output information,

f. input information, and

g. any combination of a through f.

53. A control system for executing an application program and evaluating the accuracy of input/output information comprising:

a. a plurality of main processor modules, each executing said application program;

b. at least one field input/output module communicating with each main processor module; and

c. a voting system for comparing information between said main processor modules.

54. A control system for executing an application program comprising:

a. a plurality of main processor modules;

b. at least one field input/output module communicating with each main processor module;

c. an attenuated feed back system for determining faults in main processor communications;

d. an attenuated loop back path for all channel transmission information sent over a communication channel by the transmitting processor to any other processors;

e. memory in said transmitting processor for storing the loop-back information received over said attenuated loop-back path;

f. a comparison system for comparing the channel transmitted information with the loop back information stored in memory;

g. apparatus for storing a fault code where said channel transmitted information does not compare to said loop back information;

h. a comparison system for comparing the loop-back information stored in said memory with the information as transmitted to other processors which is retransmitted to said transmitting processor ;

i. a comparison system for comparing the retransmitted information with the loop back information stored in memory; and

j. apparatus for storing a fault code where said retransmitted information does not compare to said loop back information.

55. A control system platform for executing an application program comprising:

a. a plurality of main processor modules;

b. at least one field input/output module communicating with each main processor module; and

c. a common housing form for enclosing each main processor module, having a plurality of indicators for indicating the status of each processor.

56. A channel transmission validity testing system for each processor comprising:

a. an attenuated loop back path for all channel transmission information sent over a communication channel by the transmitting processor to any other processors;

b. memory in said transmitting processor for storing the loop-back information received over said attenuated loop-back path;

c. a comparison system for comparing the channel transmitted information with the loop back information stored in memory; and

d. apparatus for storing fault code information when said channel transmitted information does not compare to said loop back information.

57. A control system platform for executing a application program comprising:

a. at least one main processor module;

b. at least one field input/output module communicating with said main processor module; and

c. a configurable housing for enclosing said main processor module and said input/output module, having a plurality of indicators for indicating the status of each module.

58. A controller for executing an application program to process control information related to control elements comprising:

a. a plurality of main processor modules;

b. at least one field input/output module for receiving and sending control information communicating with each main processor module;

c. a timer system for synchronizing time between said main processor module; and

d. at least one communication module for communicating with said main processor modules and external signals.

59. A controller for executing an application program to process control information related to control elements comprising:

a. a plurality of main processor modules;

b. a plurality of communication modules for communicating with said main processor modules and said input/output module;

c. a timer system for synchronizing time between said main processor module; and

d. at least one redundant field input/output module having a plurality of field interconnections for receiving and sending control information communicating with each main communication module.

60. A time synchronization system for each processor of a plurality of processors for synchronizing the time clocks of said main processor modules comprising:

a. apparatus for sending a rendezvous signal to all other processors;

b. apparatus for receiving a rendezvous signal from all other processors;

c. a system for determining the clocking midpoint of all processor signals;

d. a clock update apparatus which sends update signals to the clock to increase the clock rate if slower than the clocking midpoint; and

e. a clock update apparatus which sends update signals to the clock to decrease the clock rate if faster than the clocking midpoint.

61. A time synchronization system in a synchronized control system comprising:

a time synchronizing system as described in claim 60 wherein said rendezvous signals are sent during a scan cycle and said update signal occurs at least once during each scan cycle.

62. A time synchronization system as described in claim 61 further comprising a synchronized control system comprising a plurality of communication modules each module communicating independently with said processor.

63. A synchronized control system as described in claim 62 further comprising a plurality of input/output modules for communicating with the control field and said main processors and said input/output module.

64. A synchronized control system as described in claim 63 wherein there are a plurality of communication modules each module communicating independently with said processors and said input/output module.

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65 ~~66.~~ A synchronized control system as described in claim 63 further comprising a plurality of redundant input/output modules for communicating with the control field and said communication modules.

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67. A synchronized control system as described in claim 63, wherein said main processor module includes:

a. a main processor section having a program executive which runs said control system; and

b. an input/output section having a program executive for management of input output functions.

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68. A synchronized control system as described in claim 63, wherein said main processor module includes a time synchronization system which compares time between a separate time base and each main processor time and increments or decrements time by a pre-determined amount until the time for each processor matches said time base.

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69. A voting system which exchanges information between selected ones of said main processor modules of said plurality of modules and compares the information in each main processor module with the information in other selected ones of said main processor modules comprising:

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a. an apparatus for loading control system related information from each processor for storage in every other processor;

b. a comparison apparatus for comparing loaded control system related information with the comparing processor's control system information;

c. memory for storing the results of said comparison;

d. a selection apparatus for determining which loaded information compares with said comparing processor's information; and

e. a default apparatus for storing a default indication where the comparing processor's information fails to compare with a majority of said loaded processor information.

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70. A time synchronizing system as described in claim 60 wherein said rendezvous signals are sent during a scan cycle and said update signal occurs at least once during each scan cycle.

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71. A control system for executing an application program and evaluating the accuracy of input/output information comprising:

a. a plurality of main processor modules;

b. at least one field input/output module communicating with each main processor module; and

c. a voting system for comparing information between said main processor modules.

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71 ~~73~~. A control system for executing an application program comprising:

a. a plurality of main processor modules,

b. at least one field input/output module communicating with each main processor module; and

c. a attenuated feed back system for determining faults in main processor communications.

72 ~~74~~. A control system platform for executing an application program comprising:

a plurality of main processor modules;

a. at least one field input/output module communicating with each main processor module; and

b. a common housing for enclosing each main processor module; having a plurality of indicators for indicating the status of each processor.

73 ~~75~~. A control system platform for running a control system program which processes information related to a control system; said control system platform comprising:

a. a plurality of processors each executing said control system program and processing said control system information;

b. at least one input/output module for sending and receiving said information related to said control system communicating with said plurality of processors; and

c. a validation system for evaluating said control system information to be processed by said control system program prior to processing by said control system program.

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76. A control system platform for running a control system program which processes information related to a control system; said control system platform comprising:

a. a plurality of processors each executing said control system program and processing said control system information;

b. at least one input/output module for sending and receiving said information related to said control system; communicating with each of said processors;

c. at least one communication module for receiving external signals and exchanging external signals with each of said processors and external signals ; and

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d. a validation system for evaluating said control system information to be processed by said control system program prior to processing by said control system program.

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77. A control system platform for running a control system program which processes information related to a control system; said control system platform comprising:

a. a plurality of processors executing said control system program and processing said control system information said processors mounted to a common power rail;

b. at least one input/output module for sending and receiving said information related to said control system; communicating with each of said processors mounted to said common power rail communicating with said plurality of processors;

c. at least one communication module for receiving external signals and exchanging external signals with each of said processors and external signals; mounted to said common power rail communicating with said plurality of processors over a communications bus;

d. a validation system on each processor for evaluating said control system information to be processed by said control system program prior to processing by said control system program; said evaluation system comparing categories of information stored in memory on each processor with the same category of information in memory on other processors and selecting

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information on which a majority of processors compare as valid information and storing said valid information into the memory of any processor for which the information did not compare with the majority of processors.

e. each of said processors being interconnected on an inter-processor bus through a loop-back path; said loop back path applying the signals for transmitting information by each transmitting processor to other processors on said bus as an attenuated loop-back signal to said transmitting processor;

f. a storage area in the transmitting processor memory for storing said loop-back information; and

g. a comparator for comparing signals transmitted by said other processors on said bus with said loop back signals to determine if the information in said loop-back signals is the same as the signals transmitted by said other processors.

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~~78~~. A system for determining the validity of transmitted information on a control system platform bus comprising:

a. an attenuated loop-back path attached to said bus which communicates transmitted information to a transmitting processor transmitting said information over said bus;

b. capture registers resident in said transmitting processor for capturing said loop back information in said memory;

c. a comparator for comparing said attenuated loop back information captured in memory with the information transmitted by said transmitting processor;

d. a plurality of capture registers resident in said transmitting processor for capturing received information related to said information transmitted from other processors on said bus by said transmitting processor; and

e. a comparator for comparing said attenuated loop back information captured in memory with the information received by said transmitting processor from other processors on said bus.

77
~~79~~. An enclosure for circuit boards comprising:

a. a cover; having a face plate which receives an outer cover having indicia thereon identifying the circuit board functions;

b. a base; having fasteners for connecting said base to said cover; said base having a plurality of openings for receiving connectors for interconnecting said circuit boards to external connectors;

c. an unitary elongated fastener which is rotatably received in said enclosure for mounting and removing said enclosure.

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~~80~~. An enclosure as described in claim 77 ~~79~~ wherein said enclosure circuit boards comprise

a. a separate power circuit board; and

b. a separate function circuit board interconnected at one end to said power circuit board and received within said enclosure and mounted thereto.

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~~81~~. An enclosure as described in claim 78 ~~80~~ wherein said power circuit board and said function circuit board each have elongated ground pins extending through said base and disposed in a pattern such that said ground pins are received by a mating ground receptacle in a predetermined mounting position.

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~~82~~. An enclosure as described in claim 77 ~~79~~ further comprising a detector for sensing the position of said elongated fastener when the same is rotated.

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~~83~~. An enclosure as described in claim 80 ~~82~~ wherein said elongated fastener includes a characteristic which changes position when the same is rotated and said detector senses the change of position of said characteristic.

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~~84~~. An enclosure for control system circuit boards comprising:

a. a cover; having heat dissipation surface and including a face plate which receives an outer cover having indicia thereon identifying the circuit board functions and a plurality of openings to permit a plurality of LED indicators to be visible through said cover;

b. a base, having heat dissipation surface and including fasteners for connecting said base to said cover; said base having a plurality of openings for receiving connectors for interconnecting said circuit boards; and

c. a single elongated fastener which is rotatably secured in said enclosure for mounting and removing said enclosure.

83 ~~85~~. An enclosure as described in claim 82 ~~84~~ wherein said heat dissipating means includes a finned surface on said cover and said base.

84 ~~86~~. An enclosure as described in claim 82 ~~84~~ further comprising at least one thermal conductive medium adjacent to an inner surface of said enclosure.

85 ~~87~~. An enclosure as described in claim 82 ~~84~~ wherein said enclosure receives at least one circuit board and said circuit board is coupled to elongated grounding pins mounted to said enclosure which extend beyond connectors coupled to said circuit board.

86 ~~88~~. An enclosure as described in claim 85 ~~87~~ wherein there are a plurality of circuit boards received by said enclosure further comprising at least one power board and at least one function board, said at least one power board and at least one function board interconnected at one end received within said enclosure and mounted thereto.

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87 ~~89~~. An enclosure as described in claim 86 ~~88~~ wherein said power circuit board and said function circuit board each are electrically coupled to elongated ground pins extending through said enclosure and disposed such that said ground pins can only be inserted into a ground receptacle in a single position.

88 ~~90~~. An enclosure as described in claim 85 ~~88~~ further comprising an elongated fastener rotatably attached to said housing and a detector for sensing the position of said elongated fastener when the same is rotated.

89 ~~91~~. An enclosure as described in claim 82 ~~84~~ wherein said elongated fastener includes a characteristic which changes position when the same is rotated and said detector senses the change of position of said characteristic.

90 ~~92~~. A method for determining the validity of transmitted information on a bus in a multiple processor system comprising the steps of:

a. transmitting a category of information from a first processor on said bus to a second processor on the bus

b. passing said transmitted information through an attenuated loop-back path to said first processor;

c. capturing said transmitted loop-back information in said first processor memory;

d. comparing said attenuated loop back information captured in said first processor memory with the information transmitted by said first processor;

e. storing a first result of said comparing in said first processor's memory;

f. faulting the first processor when the first result indicates a difference in said transmitted information and said loop-back information;

g. capturing information which is received by said first processor from a second processor on said bus in said first processor memory;

h. comparing the captured information from said second processor with the same category of information in said first processor memory; and

i. faulting the first processor when the second result indicates a difference in said information.

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91

~~93~~. A method for determining the voting mode of a plurality of processors each having memory and coupled to a inter processor bus comprising the steps of:

a. exchanging information with said plurality of processors over said bus transmitting a category of information from a first processor on said bus to a second processor on the bus

b. passing said transmitted information through an attenuated loop-back path to said first processor;

c. capturing said transmitted loop-back information in said first processor memory;

d. comparing said attenuated loop back information captured in said first processor memory with the information transmitted by said first processor;

e. storing a first result of said comparing in said first processor's memory;

f. faulting the first processor when the first result indicates a difference in said information;

g. capturing second processor information which is received by said first processor from a second processor on said bus in said first processor memory;

h. comparing said second processor captured information with the same category of information in said first processor;

i. faulting the second processor when the second result indicates a difference in said information; and

j. reconfiguring said system to perform comparison with memory information from other processors without using faulted processors.

92
~~94~~. A method of voting between a plurality of processors having memory comprising the steps of:

a. exchanging information between said processors;

b. comparing information in selected categories in each processor, with the information received from other processors in the same selected category;

c. determining if said information conforms in a majority of processors in said category; and

d. restoring said conformed category of information in all non-conforming processors.

93 92
~~95~~. A method of voting as described in claim ~~94~~ comprising the following additional step of determining a midpoint value where three processors are voting analog input information.

94 92
~~96~~. A method of voting as described in claim ~~94~~ comprising the following additional step of determining a majority value where three processors are voting discrete input information.

95 92
~~97~~. A method of voting as described in claim ~~94~~ comprising the following additional step of determining an average value where two processors are voting analog input information.

96 92
~~98~~. A method of voting as described in claim ~~94~~ comprising the following additional step of determining a unanimous value where two processors are voting discrete input information.

97
~~99~~. A method of synchronizing time within each processor comprising the steps of:

a. sensing a synchronization signal from each synchronizing processor;

b. determining which synchronizing processor synchronization signal occurs at the midpoint of time;

c. selecting the midpoint synchronizing processor time base;

d. incrementing the rate of clocking of the latest synchronizing processor time base by a selected number; and

e. decrementing the rate of clocking of the earliest synchronizing processor by a selected number.

98 ~~100~~. A method of synchronizing time as described in claim 97 ~~99~~ wherein said processor has a predetermined scan rate and said method is repeated for each scan.

99 ~~101~~. A method of synchronizing time as described in claim 97 ~~99~~ wherein said selected number is a predetermined time increment.

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100 ~~102~~. A method of synchronizing time in each of a plurality of main processors for synchronizing the time clocks of said main processor modules the steps comprising the steps of:

a. sending a rendezvous signal to all other main processor modules;

b. receiving a rendezvous signal from all other main processor modules,

c. determining the clocking midpoint of all processor signals;

d. determining the clock which is late and adjusting said clock to increase the clock rate if earlier than the clocking midpoint; and

e. determining the clock which is early and adjusting said clock to decrease the clock rate if later than the clocking midpoint.

101 ~~103~~. A time synchronizing method as described in claim 100 ~~102~~ wherein said rendezvous signals are sent during a scan cycle and said adjusting step occurs at least once during each scan cycle.

102 ~~104~~. A method of testing information in a plurality of processors for accuracy, the steps comprising:

a. loading control system related information from each processor for storage in every other processor;

b. comparing said loaded control system from other processors with related information with the comparing processor's control system information;

c. storing the results of said comparison in memory;

d. determining which loaded information compares with said comparing processor's information; and

e. storing a status indication where the comparing processor's information fails to compare with a majority of said loaded processor information.

103 ~~105~~. A method as described in claim 102 ~~104~~ further comprising the following steps:

a. transmitting information on a bus from the testing main processor module to other main processor modules;

b. sampling the information transmitted;

c. comparing the sample with the information transmitted;

d. setting a fault indication if the information transmitted does not compare with the information sampled;

e. removing the processor having a fault indication from operation; and

f. reconfiguring the plurality of main processor modules to operate without said faulted processor.

104 ~~106~~. A method for channel transmission validity testing system in each processor comprising the following steps:

a. transmitting information from a transmitting processor to at least one receiving processor on channel;

b. sending such information through an attenuated loop back path to said transmitting processor;

c. comparing the channel transmitted information with the loop back information stored in memory; and

d. storing a fault code where said channel transmitted information does not compare to said loop back information.

105 ~~107~~. A channel transmission validity testing system in each processor comprising:

a. an attenuated loop-back path for all channel transmission information sent over a communication channel by the transmitting processor to any other processors;

b. memory in said transmitting processor for storing the loop-back information received over said attenuated loop-back path;

c. a comparison system for comparing the channel transmitted information with the loop-back information stored in memory;

d. apparatus for storing a fault code where said channel transmitted information does not compare to said loop-back information;

e. a comparison system for comparing the loop-back information stored in said memory with the information as transmitted to other processors which is retransmitted to said transmitting processor;

f. a comparison system for comparing the retransmitted information with the loop-back information stored in memory; and

g. apparatus for storing a fault code where said retransmitted information does not compare to said loop-back information.

Respectfully submitted,

Henry G. Kohlmann

Registration Number 20,322

EXPRESS MAIL CERTIFICATION DATE OF DEPOSIT February 27, 2001

I hereby certify that the attached correspondence is being deposited with the United States Postal Service as Express Mail Post Office to Addressee service pursuant to 37 CFR § 1.10, Express Mail No. EL608985713US on February 27, 2001, postage prepaid and is addressed to The Assistant Commissioner for Patents, Box PCT Washington, DC 20231.

Date: February 27, 2001